

82. A method according to claim 66 wherein said silicon nitride film is in contact with  
~~said semiconductor film~~

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be teach

83. A method according to claim 72 wherein said silicon nitride film is in contact with  
said semiconductor film.--

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this allowed 83

### REMARKS

The Official Action dated October 4, 1999 has been received and its contents carefully noted. Claims 19-77 were pending in the present application prior to the above amendment. New claims 78-83 have been added to recite additional protection to which Applicants are entitled. Accordingly, claims 19-83 are pending in the subject application and, for the reasons set forth in detail below, are now believed to be condition for allowance.

The Official Action initially rejects claims 29-39, 42, 43, 46, 47, 54-59 and 66-71 under 35 U.S.C. §103 as being unpatentable over Zhang (U.S. Patent No. 5,403,772) in view of Masumo (U.S. Patent No. 5,306,651). This ground of rejection is traversed for the reasons set forth below.

The present invention is related to a method for crystallizing a semiconductor film. In the claimed method, the semiconductor film is formed in contact with a silicon nitride film. The semiconductor film is then crystallized so as not to have a (111) plane orientation. Although the Zhang reference teaches, in the fifth embodiment, that a silicon oxide film or a silicon nitride film "122" is formed by sputtering on a silicon film and then crystallizing the silicon film by heating, the Zhang reference clearly fails to disclose the non-(111) plane orientation set forth in the present invention. In addition, please note that the Zhang reference discloses not only the silicon nitride film, but also the use of a silicon oxide film. Conversely, the instant specification discloses, on page 3, lines 1-3, that a TFT having a channel forming region having a (111) plane orientation tends to have a threshold voltage  $V_{th}$  shifted to a negative value. If a N-channel TFT has a large negative  $V_{th}$  value, the N-channel TFT becomes ON-state between a source region and a drain region, even if a gate voltage is not applied to the N-channel TFT. Likewise, if a P-channel TFT has a large negative  $V_{th}$  value, the P-channel TFT does not operate unless a large negative gate voltage is applied to the P-channel TFT. The method disclosed in the Zhang reference fails to recognize or eliminate these

problems. The recognition of a problem which was previously not known has been held sufficient to render claims directed to the solution to the problem unobvious. "If, as Appellants claim, there is no evidence of record that a person of ordinary skill in the art at the time of applicants' invention would have expected the problem of a large negative  $V_{th}$  value to exist at all, it is not proper to conclude that the invention which solves this problem, which is claimed as an improvement of the prior art device, would have been obvious to that hypothetical person of ordinary skill in the art." *In re Nomiya, Kohisa, and Matsumura*, 184 U.S.P.Q. 607, 612 (C.C.P.A. 1975).

Without any evidence that the problem was known in the art at the time of the Applicants' invention, there is no reason or motivation for one of skill to apply their skill to its solution. Specifically, the Zhang reference fails to even disclose a semiconductor device having a given  $V_{th}$  value. As a result, it does not provide any suggestion of the problems associated with utilizing a non-(111) plane orientation suitable for solving the problem of a large negative  $V_{th}$  value.

The Zhang reference also fails to disclose the claimed method step of crystallizing the silicon film by using a metal such as nickel and irradiating it with visible or near infrared light. Moreover, it is well known that the field-effect mobility  $\mu$  of a N-channel transistor formed on the (111) plane of silicon is lower than that formed on the (100) plane (see Figs. 2, 4, 5, 9 and 12 of T. Sato et al., "Physical Review B", Vol. 4, No. 6, 1971, pp. 1950-1960 (the Sato article) submitted herewith in the attached Information Disclosure Statement)). Similarly, the instant specification discloses, on page 25, lines 10-14, that the field-effect mobility of a N-channel TFT is improved by applying the present invention. Such advantages are not disclosed nor fairly suggested by the cited Zhang reference.

In addition to the above-described deficiencies, the Zhang reference also fails to disclose or suggest the claimed ratio of nitrogen to silicon being 1.3 to 1.5, as set forth in claims 56, 59 and 71. This ratio is important because the charge moving along the semiconductor film is trapped to the silicon nitride film when the ratio of nitrogen to silicon is lower than 1.3 (see the instant specification at page 3, lines 17-20). Also, the Zhang reference fails to disclose a silicon oxide film or a silicon nitride film formed by a CVD method and therefore fails to disclose the presence of hydrogen in the film. It is well known that hydrogen is inherently contained in the silicon nitride film when the

silicon nitride film is formed by using a CVD method. However, the Zhang reference discloses the formation of the film by sputtering method and therefore, the film does not include hydrogen as recited in the claimed invention. The presence of hydrogen in the silicon nitride film is advantageous for contributing to terminating and compensating dangling bonds in the silicon nitride film.

The cited Masumo reference fails to remedy the deficiencies of the Zhang reference. Specifically, the Masumo reference likewise fails to disclose the non-(111) plane orientation of the present invention. The Masumo reference merely teaches a passivation film of a single layer or multi-layer formed of,  $\text{SiN}_x$  or  $\text{SiO}_x\text{N}_y$ . If the  $\text{SiO}_x$  film is used, a semiconductor film tends to be crystallized with a (111) plane orientation. The Masumo reference further fails to teach the claimed ratio of nitrogen to silicon and further fails to disclose a silicon nitride film comprising hydrogen, the advantages of which are described in detail above. The Masumo reference discloses the formation of the passivation film by not only using the CVD method but also a sputtering method. Therefore, the presence of hydrogen in the silicon nitride film may not be accomplished by Masumo.

Paragraph 5 of the Official Action rejects claims 19-28, 40, 41, 44, 45, 48-53, 60-65 and 72-77 under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki (U.S. Patent No. 5,773,327) or Takayama (U.S. Patent No. 5,843,225) or Yamazaki ('U.S. Patent No. 5,639,698) in view of Masumo. This rejection is traversed for the reasons set forth in detail below.

Contrary to the Examiner's assertions, each of the Yamazaki '327, Takayama, Yamazaki '698 and Masumo references fail to disclose or fairly suggest a silicon nitride film having a ratio of nitrogen to silicon being 1.3 to 1.5, as set forth in claims 50, 53, 65 and 77, and further fail to teach the silicon nitride film comprising hydrogen, as set forth in claims 19, 24, 60 and 72. As described above, a silicon nitride film having a ratio of less than 1.3 renders a TFT comprising the silicon nitride film poor and inferior. Further, the number of dangling bonds in the silicon nitride film increases if the ratio of nitrogen to silicon is lower than 1.3. The dangling bonds in the silicon nitride film trap the charge, thereby reducing the performance of the TFT. Since dangling bonds are terminated and compensated by hydrogen, the hydrogen is effective in preventing the charge from being trapped, thereby increasing TFT performance. None of the cited references disclose or fairly

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suggest the claim feature of a silicon nitride film including hydrogen. Accordingly, these claims are believed to be allowable over the prior art.

Paragraph 6 of the Official Action, rejects claims 19-77 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-26 of U.S. Patent No. 5,605,846 in view of Masumo and further in view of Sze (VLSI Technology). Applicants intend to submit a properly filed Terminal Disclaimer shortly hereafter, to overcome the above rejection.

In view of the above, all of the claims in this case are believed to be in condition for allowance. Should the Examiner deem that any further action by the Applicants would be desirable to place this application in even better condition for issue, the Examiner is respectfully requested to contact the undersigned.

Respectfully submitted,

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